

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1 1. (Currently Amended) A multiprocessor system comprising:
2 a plurality of data processors, each data processor including:
3 a data processing core capable of data processing
4 according to program control and memory access,
5 a memory forming a local portion of a unified memory
6 shared among said plurality of data processors, and
7 a global memory arbitration logic connected to said data
8 processing core and said memory of each of said data
9 processors, said global memory arbitration logic having a
10 close connection to said data processing core of said
11 corresponding data processor and to said data processing core
12 of at least one other data processor but less than all other
13 data processors and a far connection to said data processing
14 core of additional data processors, said global memory
15 arbitration logic arbitrating access to said ~~else~~ memory
16 forming said local portion of said unified memory granting a
17 first type access to ~~else~~ said data processing cores having
18 said close connection and a second type access different from
19 ~~aid~~ said first type access to ~~far~~ said data processing cores
20 having said far connection.

1 2. (Currently Amended) The multiprocessor system of claim 1,
2 wherein:
3 said local portion of said unified memory of each data
4 processor is a dual port memory having a first port and a second
5 port; and
6 said global memory arbitration logic arbitrating access to
7 said first port of said dual port memory among said ~~else~~ data

8 processing cores having said close connection thereby providing
9 said first type access and arbitrating access to said second port
10 of said dual port memory among said ~~far~~ data processing cores
11 having said far connection thereby providing said second type
12 access.

Claims 3 and 4. (Canceled)

1 5. (Currently Amended) The multiprocessor system of claim 2,
2 wherein:

3 each of said data processors further includes a local memory
4 connected to said data processing core and directly accessible by
5 said data processing core and ~~not~~ neither directly connected to nor
6 directly accessible by said data processing cores of other data
7 processors.

1 6. (Currently Amended) A multiprocessor system comprising:
2 a plurality of data processors, each data processor including:
3 a data processing core capable of data processing
4 according to program control and memory access,
5 a memory forming a local portion of a unified memory
6 shared among said plurality of data processors having a first
7 port and a second port, and
8 a global memory arbitration logic connected to said data
9 processing core and said memory of each of said data
10 processors, said global memory arbitration logic having a
11 close connection to said data processing core of said
12 corresponding data processor and to said data processing core
13 of at least one other data processor but less than all other
14 data processors and a far connection to said data processing
15 core of additional data processors, said global memory
16 arbitration logic arbitrating access to said first port of

17 said dual port memory among said ~~else~~ data processing cores
18 having said close connection thereby providing a first type
19 access and arbitrating access to a said second port of said
20 dual port memory of another data processor among said data
21 processing cores having a said far connection to said global
22 memory arbitration logic of said another data processor
23 thereby providing a second type access.

Claims 7 and 8. (Canceled)

1 9. (Currently Amended) The multiprocessor system of claim 6,
2 wherein:

3 each of said data processors further includes a local memory
4 connected to said data processing core and directly accessible by
5 said data processing core and ~~not~~ neither directly connected to nor
6 directly accessible by said data processing cores of other data
7 processors.

1 10. (Currently Amended) The multiprocessor system of claim 6,
2 wherein:

3 said plurality of data processors consists of four data
4 processors;

5 said global memory arbitration logic of each data processor
6 has a close connection to its corresponding data processor and
7 ~~another~~ one other data processor and has a far connection to two
8 other data processors.